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# DATA SHEET

## CBT16213

24-bit bus exchange switch
with 12-bit output enables

Objective specification

2001 Jan 19

Philips
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# 24-bit bus exchange switch with 12-bit output enables

# CBT16213

## FEATURES

- 5 Ω switch connection between two ports
- TTL compatible control input levels
- Package options include plastic shrink small outline (SSOP) and thin shrink small outline (TSSOP)

## DESCRIPTION

The CBT16213 provides 24 bits of high-speed TTL-compatible bus switching or exchanging. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The CBT16213 operates as 24-bit bus switch or a 12-bit bus exchanger, which provides data exchanging between the four signal ports via the data-select (S0–S2) terminals.

The CBT16213 is characterized for operation from –40 to +85 °C.

## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS $T_{amb}$ = 25 °C; GND = 0 V | TYPICAL | UNIT |
|---|---|---|---|---|
| $t_{PLH}$ $t_{PHL}$ | Propagation delay An to Yn | $C_L$ = 50 pF; $V_{CC}$ = 5 V | 0.25 | ns |
| $C_{IN}$ | Input capacitance | $V_I$ = 0 V or $V_{CC}$ | 4.5 | pF |
| $C_{OUT}$ | Output capacitance | Outputs disabled; $V_O$ = 0 V or $V_{CC}$ | 11.5 | pF |
| $I_{CCZ}$ | Total supply current | Outputs disabled; $V_{CC}$ = 5.5 V | 3 | µA |

## ORDERING INFORMATION

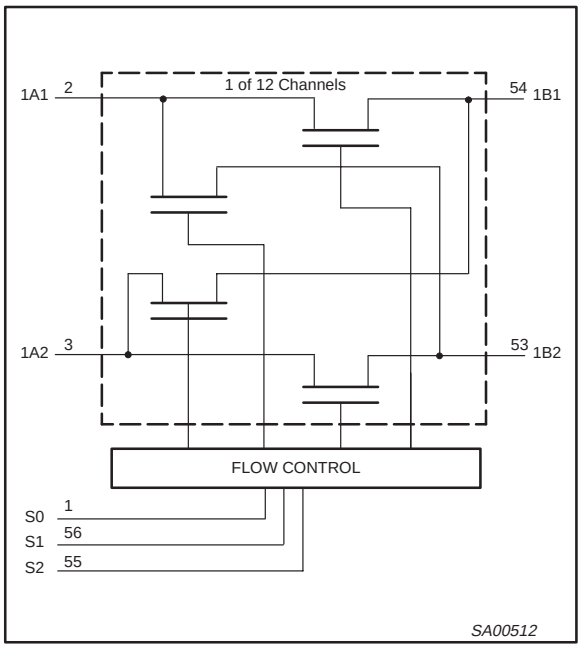
| PACKAGES | TEMPERATURE RANGE | OUTSIDE NORTH AMERICA | NORTH AMERICA | DWG NUMBER |
|---|---|---|---|---|
| 56-Pin Plastic SSOP Type III | –40 to +85 °C | CBT16213DL | CBT16213DL | SOT371-1 |
| 56-Pin Plastic TSSOP Type II | –40 to +85 °C | CBT16213DGG | CBT16213DGG | SOT364-1 |

## FUNCTION TABLE

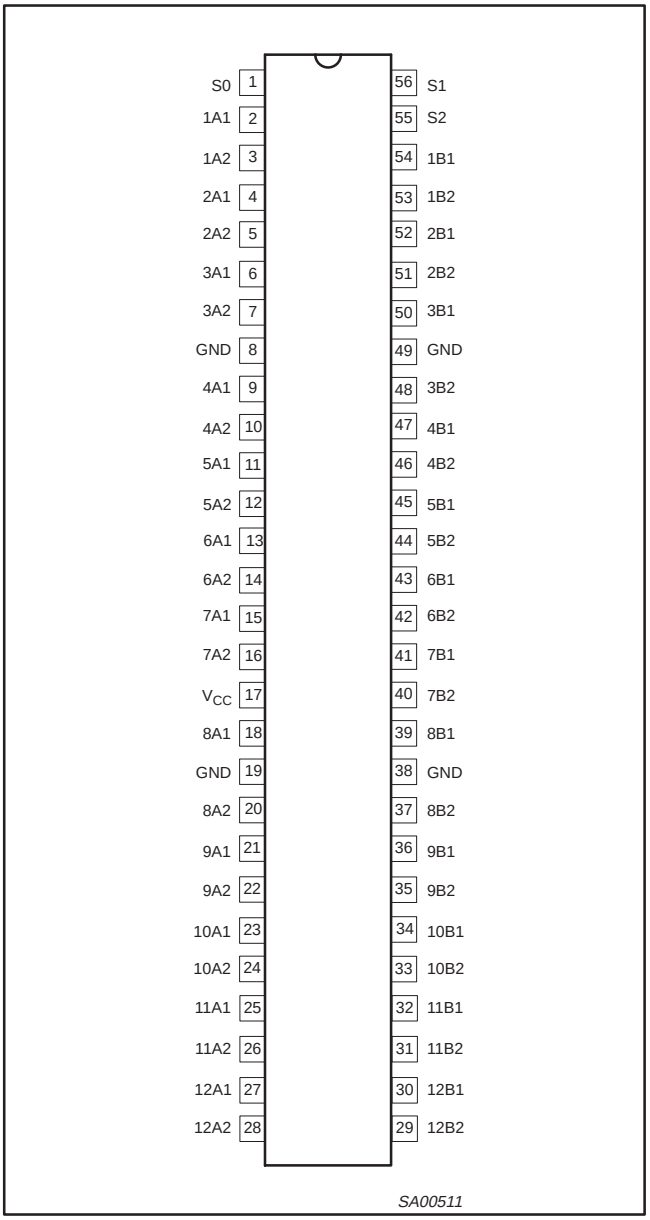
| S2 | S1 | S0 | A1 | A2 | FUNCTION |
|---|---|---|---|---|---|
| L | L | L | Z | Z | Disconnect |
| L | L | H | B1 | Z | A1 = B1 |
| L | H | L | B2 | Z | A1 = B2 |
| L | H | H | Z | B1 | A2 = B1 |
| H | L | L | Z | B2 | A2 = B2 |
| H | L | H | A2 & B2 | A1 & B2 | A1 = A2 = B2 |
| H | H | L | B1 | B2 | A1 = B1, A2 = B2 |
| H | H | H | B2 | B1 | A1 = B2, A2 = B1 |

H = High voltage level
L = Low voltage level
Z = High impedance “off” state

## LOGIC SYMBOL



## PIN CONFIGURATION




## PIN DESCRIPTION

| PIN NUMBER | SYMBOL | NAME AND FUNCTION |
|---|---|---|
| 1, 56, 55 | S0, S1, S2 | Data select |
| 2, 4, 6, 9, 11, 13, 15, 18, 21, 23, 25, 27 | 1A1–12A1 | A1 channel |
| 3, 5, 7, 10, 12, 14, 16, 20, 22, 24, 26, 28 | 1A2–12A2 | A2 channel |
| 54, 52, 50, 47, 45, 43, 41, 39, 36, 34, 32, 30 | 1B1, 12B1 | B1 channel |
| 53, 51, 48, 46, 44, 42, 40, 37, 35, 33, 31, 29 | 1B2, 12B2 | B2 channel |
| 8, 19, 38, 49 | GND | Ground (0 V) |
| 17 | $V_{CC}$ | Positive supply voltage |

## ABSOLUTE MAXIMUM RATINGS[1, 2]

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | DC supply voltage | | –0.5 to +7.0 | V |
| $I_{IK}$ | DC input diode current | $V_I < 0$ | –50 | mA |
| $V_I$ | DC input voltage[3] | | –0.5 to +7.0 | V |
| $V_{OUT}$ | DC output voltage[3] | output in Off or High state | –0.5 to +5.5 | V |
| $I_{OUT}$ | DC output current | output in Low state | 128 | mA |
| $T_{stg}$ | Storage temperature range | | –65 to +150 | °C |

**NOTES:**
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | UNIT |
|---|---|---|---|---|
| | | Min | Max | |
| $V_{CC}$ | DC supply voltage | 4.0 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2.0 | — | V |
| $V_{IL}$ | Low-level Input voltage | — | 0.8 | V |
| $T_{amb}$ | Operating free-air temperature range | –40 | +85 | °C |

## DC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | $T_{amb}$ = –40 °C to +85 °C | | | |
| | | | Min | Typ[1] | Max | |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = 4.5 V; $I_I$ = –18 mA | — | — | –1.2 | V |
| $I_I$ | Input leakage current | $V_{CC}$ = 0 V; $V_I$ = 5.5 V | — | — | 10 | μA |
| | | $V_{CC}$ = 5.5 V; $V_I$ = GND or 5.5 V | — | — | ±1 | |
| $I_{CC}$ | Quiescent supply current[2] | $V_{CC}$ = 5.5 V; $I_O$ = 0 V, $V_I$ = $V_{CC}$ or GND | — | — | 3 | μA |
| $\Delta I_{CC}$ | Additional supply current per input pin[2] | $V_{CC}$ = 5.5 V, one input at 2.7 V, other inputs at $V_{CC}$ or GND | — | — | 2.5 | mA |
| $C_I$ | Control pins | $V_I$= 3 V or 0 V | — | 4.5 | — | pF |
| $C_{IO(OFF)}$ | Power-off leakage current, B port | $V_O$ = 3 V or 0 V; S0, S1, or S2 = $V_{CC}$ | — | 11.5 | — | pF |
| | Power-off leakage current, A port | | — | 11.5 | — | pF |
| $r_{on}$[3] | A to B or B to A | $V_{CC}$ = 4.0 V; $V_1$ = 2.4 V; $I_I$ = 15 mA | — | 14 | 21 | Ω |
| | | $V_{CC}$ = 4.5 V; $V_1$ = 0 V; $I_I$ = 64 mA | — | 5 | 7 | |
| | | $V_{CC}$ = 4.5 V; $V_1$ = 0 V; $I_I$ = 30 mA | — | 5 | 7 | |
| | | $V_{CC}$ = 4.5 V; $V_1$ = 2.4 V; $I_I$ = 15 mA | — | 8 | 15 | |
| | A1 to A2 | $V_{CC}$ = 4.0 V; $V_1$ = 2.4 V; $I_I$ = 15 mA | — | 22 | 33 | |
| | | $V_{CC}$ = 4.5 V; $V_1$ = 0 V; $I_I$ = 64 mA | — | 10 | 14 | |
| | | $V_{CC}$ = 4.5 V; $V_1$ = 0 V; $I_I$ = 30 mA | — | 10 | 14 | |
| | | $V_{CC}$ = 4.5 V; $V_1$ = 2.4 V; $I_I$ = 15 mA | — | 16 | 22 | |

**NOTES:**
1. All typical values are at $V_{CC}$ = 5 V, $T_{amb}$ = 25 °C
2. This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.
3. Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

## AC CHARACTERISTICS

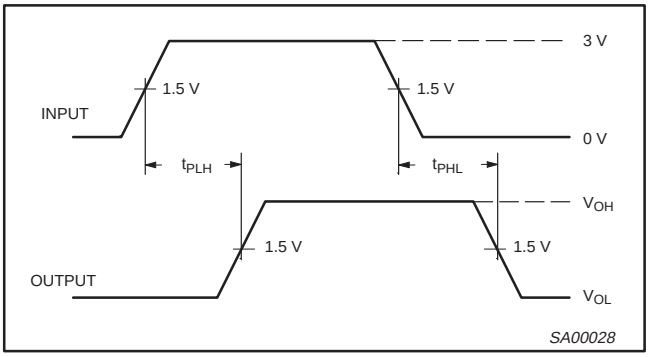
GND = 0 V; $t_R$; $C_L$ = 50 pF

| SYMBOL | PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = +5.0 V ± 0.5 V | | $V_{CC}$ = 4.0 V | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $t_{pd}$ | Propagation delay[1] | A or B | B or A | — | 0.25 | — | 0.25 | ns |
| | | A1 | A2 | — | 0.5 | — | 0.5 | ns |
| $t_{en}$ | Output enable time to High and Low level | S | A or B | 3.2 | 11.1 | — | 12.4 | ns |
| | | S0 | A2 and B2 | 4 | 10.9 | — | 13.3 | ns |
| $t_{dis}$ | Output disable time from High and Low level | S | A or B | 2.3 | 11.9 | — | 12.4 | ns |
| | | S0 | A2 and B2 | 5.7 | 12 | — | 12.8 | ns |

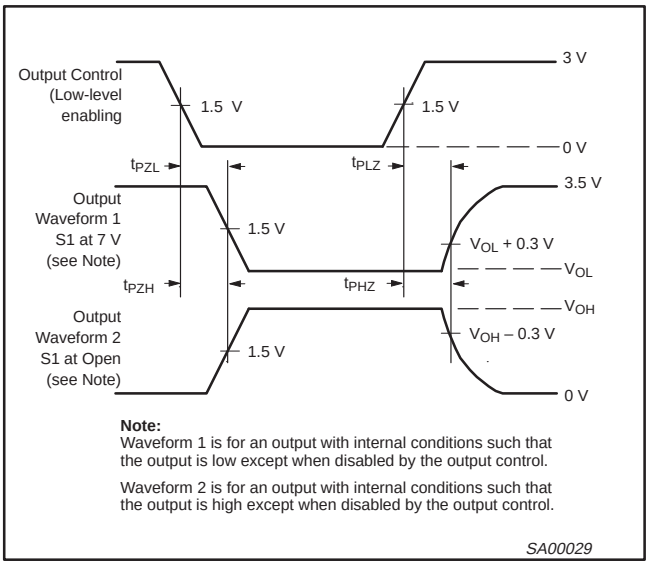
**NOTES:**
1. This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

## AC WAVEFORMS

$V_M$ = 1.5 V, $V_{IN}$ = GND to 3.0 V

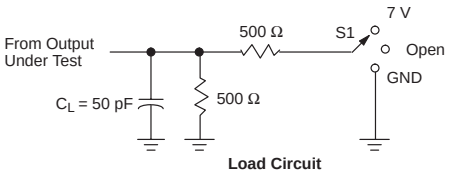



**Waveform 1. Input (An) to Output (Yn) Propagation Delays**




**Waveform 2. 3-State Output Enable and Disable Times**

## TEST CIRCUIT AND WAVEFORMS




**Load Circuit**

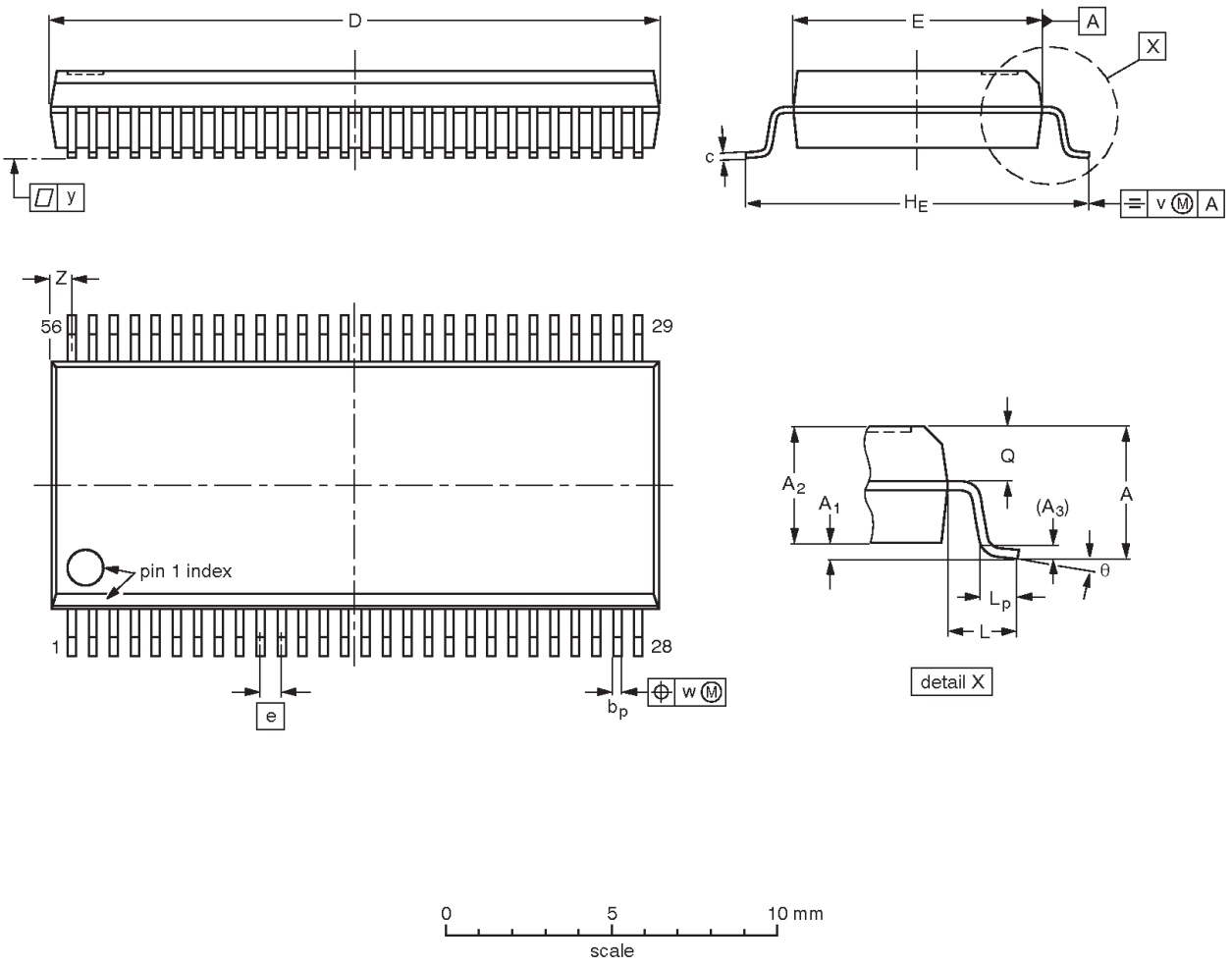
| TEST | S1 |
|---|---|
| $t_{pd}$ | open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | open |

**DEFINITIONS**

$C_L$ = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

SA00012

**SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm** **SOT371-1**




**DIMENSIONS (mm are the original dimensions)**

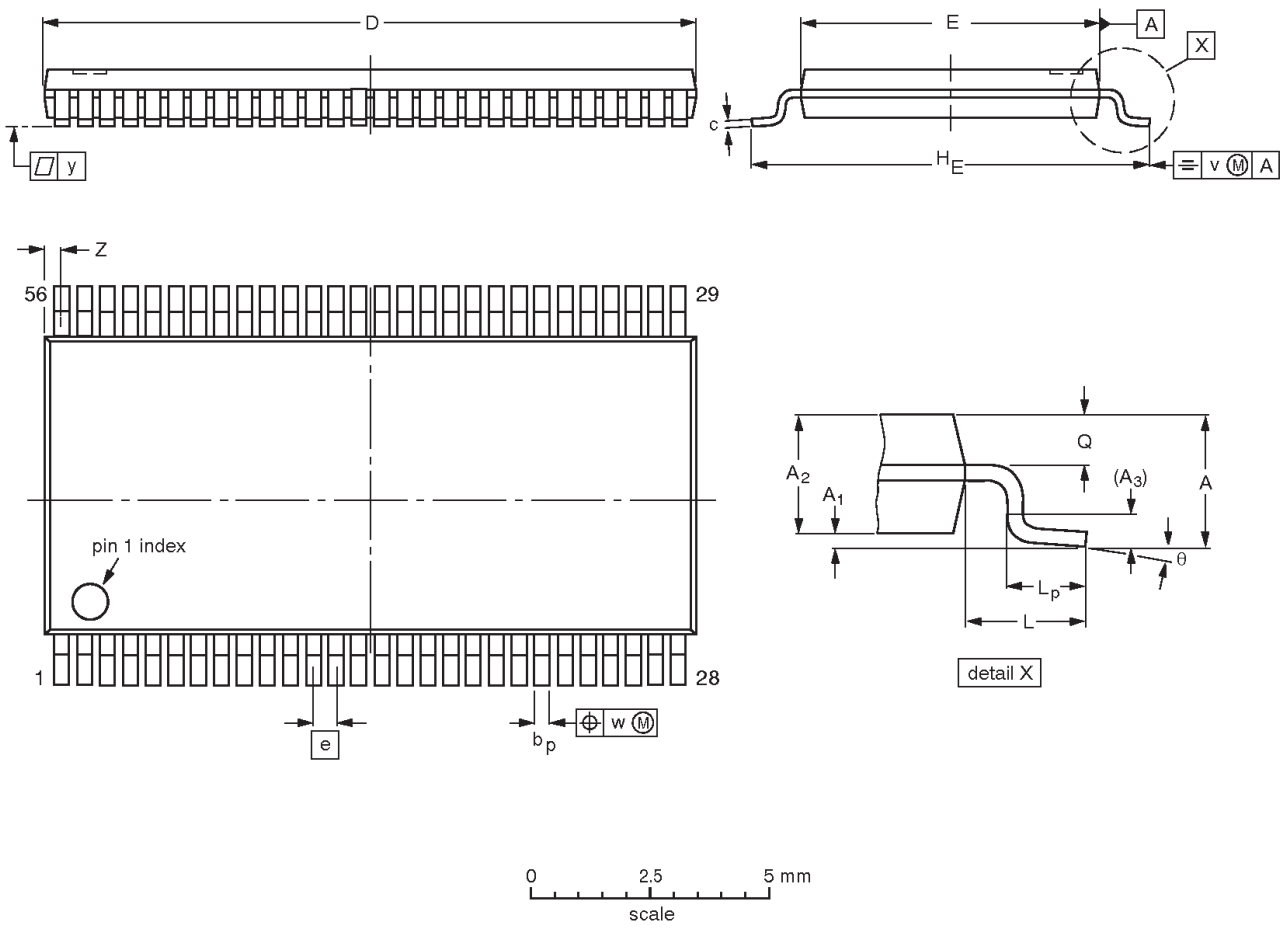
| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.8 | 0.4<br>0.2 | 2.35<br>2.20 | 0.25 | 0.3<br>0.2 | 0.22<br>0.13 | 18.55<br>18.30 | 7.6<br>7.4 | 0.635 | 10.4<br>10.1 | 1.4 | 1.0<br>0.6 | 1.2<br>1.0 | 0.25 | 0.18 | 0.1 | 0.85<br>0.40 | $8^o$<br>$0^o$ |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT371-1 | | MO-118 | | | | ~~95-02-04~~<br>99-12-27 |

**TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm SOT364-1**




**DIMENSIONS (mm are the original dimensions).**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.2 | 0.15<br>0.05 | 1.05<br>0.85 | 0.25 | 0.28<br>0.17 | 0.2<br>0.1 | 14.1<br>13.9 | 6.2<br>6.0 | 0.5 | 8.3<br>7.9 | 1.0 | 0.8<br>0.4 | 0.50<br>0.35 | 0.25 | 0.08 | 0.1 | 0.5<br>0.1 | $8^o$<br>$0^o$ |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | | |
| SOT364-1 | | MO-153 | | | | | ~~95-02-10~~<br>99-12-27 |

**NOTES**

## Data sheet status

| Data sheet status | Product status | Definition [1] |
|---|---|---|
| Objective specification | Development | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice. |
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Date of release: 01–01

Document order number:

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